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Docket No.: 1298/0F374

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Sailesh CHITTIPEDDI; Sailesh Mansinh MERCHANT

Serial No.:

Addessee" service.

09/467,253

Art Unit:

2811

Filed:

12/20/99

Examiner:

TBA

For:

WIRE BONDING METHOD FOR COPPER INTERCONNECTS IN

SEMICONDUCTOR DEVICES

Allowed:

Batch No .:

SUBMISSION OF FORMAL DRAWINGS

Hon. Commissioner of Patents and Trademarks Washington, DC 20231

Sir:

We have now procured and enclose herewith the formal drawings (5 sheets, Figures 1-5B) for this application.

Respectfully submitted,

Dated: March 1, 2001

Ya-Chiao Chang Reg. No. 43,407

Attorney for Applicant(s)

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for said storage means for preventing access to said identification devices engaged with said station means.

- 6. An identification device comprising a body; electronic memory means in said body operable for storing a unique readable code; and suitable for use with a storage system comprising a frame; a plurality of station means in said frame operable to receive said identification device; reading means operable for reading the codes of said identification device; input means operable for inputting information relating the associated code of said identification means to the associated object to said identification means and for inputting information as to a selected one of said identification devices or its associated object; processing means operable for processing inputted information to said input means; and display means responsive to said processing means and operable for indicating the location of a selected identification device engaged in one of said station means based on inputted information.
- 7. The identification device as claimed in claim 6, further comprising locking means operable for inhibiting the disengagement of said device from said station means unless'said processing means receives predetermined information from said input means.
- 8. The identification device as claimed in claim 7, wherein said locking fineans comprises a physical shape.
- 9. The identification device as claimed in claim 7, wherein said locking means comprises a notch.
- 10. In an array of electronic memory devices each having a single wire data line and a ground line and arranged for reading by designating two coordinates, the improvement

comprising interconnecting each data line to each other data line through a resistive path substantially lower than the resistance of each of said electronic memory device.

11. The array as claimed in claim 10, wherein each resistive path is about two orders of magnitude less than the resistance of said electronic memory device.